AMENDMENT

IN THE CLAIMS:

Please replace pending claims 1 and 11 with the following clean amended claims 1 and 11:

B1

1. (Amended) An integrated circuit chip comprising:

a semiconductor substrate;

a semiconductor device over said semiconductor substrate;

a dielectric layer formed over said semiconductor substrate and said semiconductor device, said dielectric layer having a channel opening and a via provided therein, said via having a via entrant angle formed from a rim of said channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said channel opening forms a collimator for said via and a depth and a cross-sectional area of the channel opening are determined by the via entrant angle;

a seed layer lining said channel opening and said via; and

a conductive layer damascened into said seed layer and said dielectric layer whereby said conductive layer in said channel opening is operatively connected by said conductive layer in said via to said semiconductor device without voids.

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11. (Amended) An integrated circuit chip comprising:

a semiconductor substrate;

a semiconductor device on said semiconductor substrate;

a first channel dielectric layer formed over said semiconductor substrate and said semiconductor device, said first channel dielectric layer having a first channel opening provided therein;

a first seed layer lining said first channel opening in said first channel dielectric layer;

a first conductive layer damascened into said first seed layer and said first channel dielectric layer whereby said conductive layer in said first channel opening is operatively connected to said semiconductor device;

second channel and via dielectric layers formed over said first channel dielectric layer, said second channel and via dielectric layers having a second channel opening

and a via provided therein, said via having a via entrant angle formed from a rim of said second channel opening to a rim of the via and a horizontal bottom of the channel opening of greater than about 69 degrees whereby said second channel opening forms a collimator for said via and a depth and a cross-sectional area of the second channel opening are determined by the via entrant angle;

B2

a second seed layer lining said second channel opening and said via; and

a second conductive layer damascened into said second seed layer and said second channel dielectric and via layers whereby said second conductive layer in said second channel opening is connected by said second conductive layer in said via to said first conductive layer in said first channel without voids.